Kindly enter the following amendments:

IN THE CLAIMS:

Please amend Claim 12 as follows:

12. (Twice Amended) A delay circuit according to claim 2, wherein the MOS capacitor is a node disposed on a transmission path of a logic signal, and is at least represented by a single p-MOS transistor whose gate is connected to a first node of the inverter chain that changes a logic level of the logic signal from a high level to a low level, and whose source and drain are fixed at a [ground]power potential.

Please add the following new claim 18:

B1 SUB C3

18. A delay circuit comprising a plurality of cascading gate circuits and a plurality of MOS capacitors connected to the output sections of said gate circuits, wherein:

all the MOS capacitors are connected so as to turn from the off-state to the on-state when the logic signal having the logic level targeted for delay is input into the head gate circuit among said cascading gate circuits.